IN THE CLAIMS

Please amend the claims as follows.

1.-12. (Canceled)

13. (Original) A device comprising:

a first supply node and a second supply node;

a plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes;

a plurality of switching units, each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes, wherein each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal; and

a redundant array for replacing at least one memory segment of the plurality of memory segments.

14. (Original) The device of claim 13 further comprising a redundancy controller connected to the switching units for selectively setting the state of the select signal based on a number of programming signals.

15. (Original) The device of claim 14 further comprising a programming unit for generating the programming signals based on a programmed address stored in the programming unit.

16. (Original) The device of claim 13, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective.

17.-47. (Canceled)

48. (Original) A device comprising:

a first supply node and a second supply node;

a plurality of memory segments, each of the memory segments including a plurality of memory cells, each of the memory cells including:

a first storage node and a second storage node;

a latch connected to the first and second storage node and connected in between a first internal node and a second internal node;

a first access element for accessing the first storage node; and

a second access element for accessing the second storage node;

a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments; and

a plurality of second switching units, each of the second switching units connecting between the second supply node and one of the memory segments.

49. (Original) The device of claim 48, wherein at least one of the memory segments is defective.

50. (Original) The device of claim 48, wherein at least one of the memory segments has a circuit short between the first and second internal nodes

51. (Original) The device of claim 48, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective.

52. (Original) The device of claim 48, wherein in each of the memory segments, the plurality of memory cells are arranged in a plurality of rows connected in parallel between one of the first switching unit and one of the second switching units.

53. (Original) The device of claim 48, wherein each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments.

54. (Original) The device of claim 48, wherein each of the second switching units includes a transistor having a source and a drain connected between the second supply node and one of the memory segments.

55. (Original) The device of claim 48, wherein the latch includes:

a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and

a second inverter having an input node connected to the second storage node and an output node connected to the first storage node.

56. (Original) The device of claim 55, wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line.

57. (Original) The device of claim 48, wherein the latch includes:

a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and

a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node.

58. (Original) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a supply node for providing a voltage source;

a memory array connected to the supply node via a supply path for receiving the voltage source;

a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory segment is defective; and

a redundant array for replacing the memory segment if the memory segment is defective.

59. (Original) The system of claim 58, wherein memory array includes a plurality of memory segments connected in parallel with each other, each of the memory segments connecting in series with the supply control circuits and the supply node.

60. (Original) The system of claim 59, wherein at least one of the memory segments is defective.

61. (Original) The system of claim 59, wherein the supply control circuit includes a plurality of switching units, each of the switching units connecting in series with one of the memory segments and the supply node.

62. (Original) The system of claim 58 further comprising a redundant array for replacing the memory segment if the memory segment is defective.

63. (Original) A method comprising:

determining a condition of a memory device;

isolating a memory segment of the memory device from a supply source if the memory segment is defective; and

replacing the memory segment with a redundant segment if the memory segment is defective.

64. (Original) The method of claim 63, wherein determining a condition of a memory device includes detecting for a defect in a memory array of the memory device.

65. (Original) The method of claim 63, wherein isolating the memory segment includes electrically disconnecting the memory segment from the supply source.

66.-75. (Canceled)

76. (Previously Presented) The device of claim 13, wherein the memory segments include a number of static random access memory (SRAM) cells.

77. (Previously Presented) The system of claim 58, wherein the memory segment includes a number of static random access memory (SRAM) cells.

[[76.]] 78. (Currently Amended) The method of claim 63, wherein isolating the memory segment includes isolating a number of static random access memory (SRAM) cells from the supply source.